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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,815	09/28/2000	Gregory A. Overkamp	10559/274001/P9281-ADI	9785

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,815	OVERKAMP ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- Th MAILING DATE of this communication appears on th cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ___ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "loading the plurality of instructions into a register, said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources" (in claims 1, 9, 14, and 19) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Note Fig. 5 shows a plurality of instruction sources, 506, 510, 515, and 520. However, it does not show **a register** receiving instructions from the instruction sources.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-15, and 17-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Favor et al. (U.S. Patent No. 5,809,273) (Hereafter referred to as Favor et al.'273).

Referring to claim 1, Favor et al.'273 discloses, as claimed, a method of handling a plurality of instructions within a processor (microprocessor 120, See Fig. 1) comprising: loading the plurality of instructions into a register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions), said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources (main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2); determining (by predecoder 270, see Fig. 2) the number and size of the plurality of instructions

(see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction bytes to determine the length of each instruction and therefore the number of instructions once the instruction boundaries are known); and decoding (by such as instruction decoder 220, see Fig. 2, and col. 3, lines 25-27, regarding instructions are decoded in parallel) the plurality of instructions.

Referring to claim 9, Favor et al.'273 discloses, as claimed, a method of decoding a plurality of instructions within a processor (microprocessor 120, See Fig. 1) comprising: determining the size of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction); loading the plurality of instructions into an instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions), said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources (main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2); presenting the plurality of instructions from

the instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions) to a decoder (instruction decoder 220, see Fig. 2); and decoding (by such as instruction decoder 220, see Fig. 2, and col. 3, lines 25-27, regarding instructions are decoded in parallel) each of the plurality of instructions within a single clock cycle (see col. 3, lines 19-21, regarding multiple instructions are decoded per cycle).

Referring to claim 14, Favor et al.'273 discloses, as claimed, a processor (microprocessor 120, See Fig. 1) comprising: an instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions) capable of holding a plurality of instructions, said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources (main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2); one or more pre-decoders (predecoder 270, see Fig. 2) which determines the size and number of the plurality of instructions (see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction

bytes to determine the length of each instruction and therefore the number of instructions once the instruction boundaries are known); and a decoder (instruction decoder 220, see Fig. 2, and col. 3, lines 25-27, regarding instructions are decoded in parallel) which substantially simultaneously receives the plurality of instructions from the instruction register (see col. 3, lines 25-27, regarding instructions are decoded in parallel), wherein the decoder decodes each of the plurality of instructions within a single clock cycle (see col. 3, lines 19-21, regarding multiple instructions are decoded per cycle).

Referring to claim 19, Favor et al.'273 discloses, as claimed, an apparatus (microprocessor 120, See Fig. 1), including instructions residing on a machine-readable storage medium (main memory 130, see Fig. 1), for use in a machine system to handle a plurality of instructions, the instructions causing the machine to: determine (by predecoder 270, see Fig. 2) the size of the plurality of instructions (see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction bytes to determine the length of each instruction and therefore the number of instructions once the instruction boundaries are known); load the plurality of instructions into an instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted

as a register since it is a fast storage device saving the instructions), said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources (main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2); present the plurality of instructions from an instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions) into a decoder (instruction decoder 220, see Fig. 2, and col. 3, lines 25-27, regarding instructions are decoded in parallel); and decode each of the plurality of instructions within a single clock cycle (see also col. 3, lines 19-21, regarding multiple instructions are decoded per cycle; and see col. 3, lines 25-27, regarding instructions are decoded in parallel).

As to claim 2, Favor et al.'273 also discloses: decoding the plurality of instructions within a single clock cycle (see also col. 3, lines 19-21, regarding multiple instructions are decoded per cycle; and see col. 3, lines 25-27, regarding instructions are decoded in parallel).

As to claim 3, Favor et al.'273 also discloses: decoding the plurality of instructions substantially simultaneously (see

also col. 3, lines 19-21, regarding multiple instructions are decoded per cycle; and see col. 3, lines 25-27, regarding instructions are decoded in parallel).

As to claim 4, Favor et al.'273 also discloses: decoding width bits to determine the size of the instructions (see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction bytes to determine the length of each instruction and therefore the number of instructions once the instruction boundaries are known).

As to claim 5, Favor et al.'273 also discloses: communicating the number and size of the plurality of instructions to the decoder (see Col. 5, lines 34-40, regarding predecoder unit 270 decodes the instruction bytes to determine the number of instructions and length of each instruction and transfer the predecode information to decoder 220).

As to claim 6, Favor et al.'273 also discloses: loading a first of the plurality of instructions having a first size (see col. 1, lines 44-47, or col. 5, lines 39-43, x86 instructions has a first size such as 4 bytes (32 bits)) and a second of the plurality of instructions having a second size (see col. 1, lines 44-47, or col. 5, lines 39-43, x86 instructions has a second size such as 2 bytes (16 bits)).

As to claim 7, Favor et al.'273 also discloses: loading a first of the plurality of instructions having a first size (see col. 1, lines 44-47, or col. 5, lines 39-43, x86 instructions has a first size such as 4 bytes (32 bits)), and loading a second and a third of the plurality of instructions having a second size (see col. 1, lines 44-47, or col. 5, lines 39-43, x86 instructions has a second size such as 2 bytes (16 bits)), wherein the first size is 32-bits and the second size is 16-bits.

As to claims 8, 13, 18, and 22, Favor et al.'273 also discloses: handling the plurality of instructions within a digital signal processor (microprocessor 120, See Fig. 1).

As to claims 10 and 20, Favor et al.'273 also discloses: simultaneously presenting each of the plurality of instructions to the decoder (see also col. 3, lines 19-21, regarding multiple instructions are decoded per cycle; and see col. 3, lines 25-27, regarding instructions are decoded in parallel).

As to claims 11, 15, and 21, Favor et al.'273 also discloses: decoding the plurality of instructions to determine the width of the plurality of instructions (see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction bytes to determine the length of each instruction and therefore the

number of instructions once the instruction boundaries are known).

As to claim 12, Favor et al.'273 also discloses: loading (from main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2) a next plurality of instructions into the single instruction register (instruction cache 214, see Fig. 2).

As to claim 17, Favor et al.'273 also discloses: the pre-decoder (predecoder 270, see Fig. 2) communicates the number and size of the plurality of instructions to the decoder (see Col. 5, lines 34-40, regarding predecoder unit 270 decodes the instruction bytes to determine the number of instructions and length of each instruction and transfer the predecode information to decoder 220).

Response to Arguments

4. Applicant's arguments mailed 12/2/04 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the drawings problems, Applicant's response has not completely overcome the objections.

As set forth in the art rejections above, Favor et al.'273 anticipates the claimed invention.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions

directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

January 21, 2005